WHAT IS CLAIMED IS:

1. A level shifter having an automatic delay adjusting function, comprising:

an input terminal to which an input signal having a first amplitude voltage corresponding to potential difference between a first power voltage and a given voltage is input;

a level shifting unit for level shifting said first amplitude voltage of said input signal input to said input terminal into a second amplitude voltage corresponding to potential difference between a second power voltage and said given voltage;

an output terminal for outputting an output signal resulting from shift performed by said level shifting unit; and

an automatic delay adjusting circuit for automatically correcting balance between a rise delay time and a fall delay time of said output signal that results from the shift performed by said level shifting unit and is output from said output terminal in accordance with change of a voltage value of at least one of said first power voltage and said second power voltage.

2. The level shifter having an automatic delay adjusting function of Claim 1,

wherein said automatic delay adjusting circuit compensatively increases the quantity of a current flowing to said output terminal when said rise delay time of said output signal output from said output terminal is longer than said fall delay time.

3. The level shifter having an automatic delay adjusting function of Claim 2,

wherein said automatic delay adjusting circuit includes an N-type transistor, and

said second power voltage is supplied to one end of said N-type transistor, the other end thereof is connected to said output terminal and a gate thereof is connected to said input terminal.

4. The level shifter having an automatic delay adjusting function of Claim 3,

wherein said automatic delay adjusting circuit further includes a P-type transistor, and

a drain of said P-type transistor is connected to a source of said N-type transistor, said first power voltage is supplied to a source thereof and said second power voltage is supplied to a gate thereof.

5. The level shifter having an automatic delay adjusting function of Claim 2,

wherein said automatic delay adjusting circuit includes a current mirror circuit,

said current mirror circuit includes a first N-type transistor and first and second P-type transistors,

said given voltage is supplied to a source of said first N-type transistor, a drain thereof is connected to gates of said first and second P-type transistors and a gate thereof is connected to said input terminal,

a drain of said first P-type transistor is connected to the drain of said first N-type transistor and said second power voltage is supplied to a source thereof, and

a drain of said second P-type transistor is connected to said output terminal and said second power voltage is supplied to a source thereof.

6. The level shifter having an automatic delay adjusting function of Claim 5, further comprising an inverter for inverting said signal resulting from the shift performed by said level shifting unit and for outputting an inverted signal to said output terminal,

wherein said current mirror circuit further includes a second N-type transistor, and

a source of said second N-type transistor is connected to the drain of said first N-type transistor, a drain thereof is connected to the drain of said first P-type transistor and a gate thereof is connected between said inverter and said output terminal.

7. The level shifter having an automatic delay adjusting function of Claim 1,

wherein said automatic delay adjusting circuit compensatively reduces lowering

of a voltage on the side of said input terminal of said level shifting unit or a voltage on the side of said output terminal of said level shifting unit when said rise delay time of said output signal output from said output terminal is longer than said fall delay time.

8. The level shifter having an automatic delay adjusting function of Claim 3,

wherein said automatic delay adjusting circuit includes serially connected first and second N-type transistors,

a gate of said first N-type transistor is connected to said input terminal and a drain thereof is connected to a signal input side of said level shifting unit, and

said given voltage is supplied to a source of said second N-type transistor, a drain thereof is connected to a source of said first N-type transistor and said second power voltage is supplied to a gate thereof.

9. The level shifter having an automatic delay adjusting function of Claim 7,

wherein said automatic delay adjusting circuit includes serially connected first and second N-type transistors,

a gate of said first N-type transistor is connected to a signal output side of said level shifting unit and a drain thereof is connected to said output terminal, and

a drain of said second N-type transistor is connected to a source of said first N-type transistor, said given voltage is supplied to a source thereof and said first power voltage is supplied to a gate thereof.

10. The level shifter having an automatic delay adjusting function of Claim 8,

wherein said level shifting unit is a cross latch type shifter including first and second P-type transistors and third and fourth N-type transistors,

a drain of one of said first and second P-type transistors is connected to a drain of the other P-type transistor and a drain of said second P-type transistor is connected to said output terminal,

a gate of said third N-type transistor is connected to said input terminal and said given voltage is supplied to a source thereof, and a gate of said fourth N-type transistor is connected to said input terminal through an inverter and said given voltage is supplied to a source thereof,

said automatic delay adjusting circuit includes a fifth N-type transistor, and

a drain of said fifth N-type transistor is connected to the source of said fourth N-type transistor, said given voltage is supplied to a source thereof and said second power voltage is supplied to a gate thereof.

11. The level shifter having an automatic delay adjusting function of Claim 10,

wherein said automatic delay adjusting circuit further includes a sixth N-type transistor, and

a drain of said sixth N-type transistor is connected to the source of said third N-type transistor, said given voltage is supplied to a source thereof and said first power voltage is supplied to a gate thereof.

12. The level shifter having an automatic delay adjusting function of Claim 1,

wherein said level shifting unit is a cross latch type shifter including first and second P-type transistors and first and second N-type transistors,

a drain of one of said first and second P-type transistors is connected to a gate of the other P-type transistor and a drain of said second P-type transistor is connected to said output terminal, and

a gate of said first N-type transistor is connected to said input terminal and said given voltage is supplied to a source thereof, and a gate of said second N-type transistor is connected to said input terminal through an inverter and said given voltage is supplied to a source thereof.